1. (Original) A ferroelectric memory device comprising:

a plurality of capacitor elements each formed on a semiconductor substrate and composed of a lower electrode, a capacitor insulating film made of a ferroelectric material formed on the lower electrode, and an upper electrode formed on the capacitor insulating film,

each of the lower electrode being buried in a burying insulating film to have an upper surface planarized relative to an upper surface of the burying insulating film and having a plane configuration such that a distance from an arbitrary position on the upper surface of the lower electrode to the nearest end portion thereof is about 0.6 μm or less.

2. (Original) The ferroelectric memory device of claim 1, wherein a protective film for protecting each of the lower electrodes is formed on a side surface of the lower electrode.

3. (Currently Amended) The ferroelectric memory device of claim 1, wherein each of the capacitor elements has a first contact plug formed under the lower electrode and electrically connected to the lower electrode.

4. (Original) The ferroelectric memory device of claim 3, wherein a dummy memory cell having a dummy capacitor element including a lower electrode which does not operate electrically is placed in a peripheral portion of a memory cell placement region in which the plurality of capacitor elements are placed, and

a contact plug connected to the lower electrode of the dummy capacitor element and nearly equal in configuration and material to the contact plug of each of the capacitor elements is formed under the lower electrode of the dummy capacitor element.

5. (Currently Amended) The ferroelectric memory device of claim 3, wherein a value of a ratio of a total area of the contact plugs to an area of [[the]] a memory cell placement region in which the plurality of capacitor elements are placed is about 0.3 or less.

6. (Original) The ferroelectric memory device of claim 1, wherein the lower electrode is made of platinum, iridium, ruthenium, an alloy containing at least one of platinum, iridium, and ruthenium, or an oxide of iridium or ruthenium.

7. (New) The ferroelectric memory device of claim 4, wherein the value of a ratio of a total area of the first contact plug to an area of the memory cell placement region is about 0.3 or less.

8. (New) The ferroelectric memory device of claim 1, wherein the peripheral portion of the upper surface of the lower electrode and the center portion thereof has a same height.

9. (New) The ferroelectric memory device of claim 1, wherein a recess formed between the peripheral portion of the lower electrode and the center portion thereof is 20 nm or less.